

Logic gates explained

Use this handy guide to learn how logic gates work.



Name	Diagram	Truth Table	Description															
AND		<table border="1"> <thead> <tr> <th>x</th> <th>y</th> <th>F</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	x	y	F	0	0	0	0	1	0	1	0	0	1	1	1	The AND gate requires signals from both inputs (x and y) to activate the output (F).
x	y	F																
0	0	0																
0	1	0																
1	0	0																
1	1	1																
OR		<table border="1"> <thead> <tr> <th>x</th> <th>y</th> <th>F</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	x	y	F	0	0	0	0	1	1	1	0	1	1	1	1	The OR gate requires signals from one or both inputs (x and or y) to activate the output (F).
x	y	F																
0	0	0																
0	1	1																
1	0	1																
1	1	1																
NOT		<table border="1"> <thead> <tr> <th>x</th> <th>F</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> </tr> </tbody> </table>	x	F	0	1	1	0	The NOT gate is an inverter. When it receives a signal from its input (x) it does not activate the output (F). When it doesn't receive a signal , it activates the output.									
x	F																	
0	1																	
1	0																	
Advanced gates																		
NAND		<table border="1"> <thead> <tr> <th>x</th> <th>y</th> <th>F</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	x	y	F	0	0	1	0	1	1	1	0	1	1	1	0	The NAND gate is an inverter. When it receives a signal from either or neither input (x or y) it will activate the output (F). If it receives a signal from both it will not activate the output.
x	y	F																
0	0	1																
0	1	1																
1	0	1																
1	1	0																
NOR		<table border="1"> <thead> <tr> <th>x</th> <th>y</th> <th>F</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	x	y	F	0	0	1	0	1	0	1	0	0	1	1	0	The NOR gate is an inverter. When it receives a signal from neither input (x) it will activate the output (F). If it receives any signals from either or both inputs, it will not activate.
x	y	F																
0	0	1																
0	1	0																
1	0	0																
1	1	0																
XOR		<table border="1"> <thead> <tr> <th>x</th> <th>y</th> <th>F</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	x	y	F	0	0	0	0	1	1	1	0	1	1	1	0	The XOR gate is an exclusive gate, this means it will only activate the output (F) when it receives one signal from the chosen input (x)
x	y	F																
0	0	0																
0	1	1																
1	0	1																
1	1	0																
XNOR		<table border="1"> <thead> <tr> <th>x</th> <th>y</th> <th>F</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	x	y	F	0	0	1	0	1	0	1	0	0	1	1	1	The XNOR gate is an exclusive gate, this means it will only activate the output (F) when both inputs provide a signal, or provide no signal.
x	y	F																
0	0	1																
0	1	0																
1	0	0																
1	1	1																